M.Tech (EMBEDDED SYSTEMS)
Two Year (Four Semesters)
Scheme of Instruction and Syllabus
(Grading System)

(With effect from 2013-2014 admitted batch onwards)
# COURSE STRUCTURE

## I SEMESTER

<table>
<thead>
<tr>
<th>SUBJECT CODE</th>
<th>SUBJECT NAME</th>
<th>Credit</th>
<th>Periods/Week</th>
<th>Sessional Marks</th>
<th>University Exam Marks</th>
<th>Total</th>
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<tbody>
<tr>
<td>MTES-1</td>
<td>Digital Signal Processing</td>
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<td>MTES-2</td>
<td>VLSI Design Techniques</td>
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<td>Digital System Design</td>
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<td>Elective-I</td>
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<td>MTES-7</td>
<td>HDL Programming Lab</td>
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**Elective-I**

a) EDA TOOLS

b) CPLD and FPGA Architecture and Applications

c) Digital Data Communications
### II SEMESTER:

<table>
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<tr>
<th>SUBJECT CODE</th>
<th>SUBJECT NAME</th>
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<td>Embedded Computing Systems</td>
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<td>MTES-12</td>
<td>Low Power VLSI Design</td>
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**Elective-II**

- a) System Modeling & Simulation
- b) Image Processing
- c) Computer and Communication Networks
### III SEMESTER:

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<th>Subject Code</th>
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Project work (PART-I) to be submitted before the end of 3rd Semester and it will be evaluated by a committee consisting of Chairman, Board of Studies, and Head of the Department and thesis guide.

### IV SEMESTER:

<table>
<thead>
<tr>
<th>Subject code</th>
<th>Subject title</th>
<th>Credits</th>
<th>Sessional Marks</th>
<th>University Exam marks</th>
<th>Total</th>
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<td>MTES – 18</td>
<td>Thesis (Part II)</td>
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<td>30</td>
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</table>

Thesis work is for a period of SIX months in Industry/Department. The students are required to submit their thesis two/three phases. Thesis is evaluated by a committee consisting of an external member from reputed institution, HOD, Chairman BOS and thesis Guide.
UNIT -I
Advanced digital filter design techniques: Multiple band optimal FIR filters – design of filters with simultaneous constraints in time and frequency response, Optimization methods for designing IIR filters, comparison of optimum FIR filters and delay equalized elliptic filters.

UNIT -II
Multirate DSP : The basic sample rate alteration – time – domain characterization, frequency – domain characterization: Cascade equivalences, filters in sampling rate alteration systems, digital filter banks and their analysis and applications, multi level filter banks, estimations of spectra form finite – duration observation of signals.

UNIT -III
Linear prediction and optimum linear filters: forward and backward linear prediction, AR Lattice and ARMA lattice – ladder filters, Wieners filters for filtering on prediction.

UNIT -IV
DSP Algorithms: The Goertzel algorithm, the chirp – Z transform algorithm the Levinson – Durbin algorithms, the Schur algorithm, And other algorithms, computations of the DFT, concept of tunable digital filters.

UNIT - V
Signal Processing Hardware: Multipliers, dividers, different forms of FIR Hardware, multiplexing, DTTR, TDM to FDM translator, realization of frequency synthesizer, FIET hardware realization, different FT architectures, special FFT processors, convolvers, Lincoln laboratory FDP and the compatible computer configurations.

UNIT- VI
Applications of DSP: Speech: Models of speech production, speech analysis – synthesis system vocoder analyzers and synthesizers, linear prediction of speech. DTMF System.

Text Books:
1. Theory and applications of digital signal processing by Lawrence R. Rabiner and Bernard Gold, PHI

Reference Books:
UNIT –I
INRODUCTION: Basic Principle of MOS Transistor, Introduction to Large Signal MOS Models (Long Channel) For Digital Design.

UNIT –II

UNIT –III

UNIT -IV
Sequential MOS Logic Design: Static Latches, Flip Flops and registers, Dynamic Latches and Registers, CMOS Schmitt trigger, Monostable Sequential Circuits, Astable Circuits, Memory Design, ROM and RAM Cells Design

UNIT –V
Interconnect and Clock Distribution: Interconnect Delays, Cross Talks, Clock Distribution. Introduction to Low-power Design, Input and Output Interface circuits.

UNIT –VI

TEXT BOOKS:

REFERENCE:
1. Weste and Eshraghian, “ Principles of CMOS VLSI design” Addison – Wesley, 2002
UNIT -I
Introduction to Embedded Systems, Processor and Memory Organization:
Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit. Structural units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded system, allocation of memory to program segments and blocks and memory map of a system, DMA, interfacing processor, memories and Input Output Devices.

UNIT -II
Devices and Buses for Device Drivers and Networks: I/O devices, timer and counting devices, serial communication using the ‘I2 C’, CAN and advanced I/O buses between the networked multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses. Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

UNIT -III
Programming Concepts and Embedded Programming in C and C++: Software programming in assembly language (ALP) and in high level language ‘C’, ‘C’ program elements: header and source files and preprocessor directives, program elements: macros and functions, data types ,data structures, modifiers , statements , loop and pointers, queues, stacks , lists and ordered lists, embedded programming in C++, embedded programming in java, ‘C’ program compiler and cross compiler , source code engineering tools for embedded C/C++ , optimization of memory needs.

UNIT - IV

UNIT -V
Hardware and Software Co Design – I: Embedded System project development, embedded System design and co-design issues in system development process, design cycle in the development phase for an Embedded System.
UNIT- VI
Hardware and Software Co Design – II: Use of target system or its Emulator and In-Circuit Emulator (ICE), use of Software tools for Development of an Embedded System, use of scopes and logic analyzers for System Hardware Tests.

TEXT BOOKS:
2. Embedded System Design: A Unified Hardware/Software Introduction By Frank vahid/Tony Givargis john Wiley & sons

REFERENCES:

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UNIT -I
Integrated Circuit Devices and Modeling: MOS Transistors, Advanced MOS Modeling, Bipolar Junction Transistors, Device Model Summary, and SPICE modeling parameters.

UNIT -II
Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Source Follower, Common Gate Amplifier, High Output Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response.

UNIT -III
Operational Amplifier Design and Compensation: Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

UNIT -IV

UNIT –V
Sample and Hold& Switched Capacitor Circuits: MOS Sample – and - Hold Basics, CMOS sample and Hold Circuits, Bipolar and Bi CMOS sample and holds. Basic Operation and Analysis, First – Order and Biquad Filter, Charge Injection, Switched Capacitor gain Circuits, Correlated Double - Sampling Techniques, Other Switched Capacitor Circuits.

UNIT -VI

TEXT BOOK:

REFERENCE BOOKS:
UNIT –I
**Design of Digital Systems:** ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT –II
**Sequential Circuit Design:** Design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT –III
**Fault Modeling:** Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults. **Test Generation:** Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT –IV
**Test Pattern Generation:** D – Algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT –V
**Fault Diagnosis in Sequential Circuits:** State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT –VI
**Programming Logic Arrays and Asynchronous Sequential Machine:** Design using PLA’s, PLA minimization and PLA folding. Fault models, Test generation and Testable PLA design. Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

**TEXT BOOKS:**

**REFERENCE BOOKS:**
ELECTIVE-I

ELECTRONIC DESIGN AUTOMATION TOOLS

Subject Code: MTES -6(a)  
I-Semester  
Common with M.Tech (VLSI (MTVL-6 (C)))

Credits: 4  
Max. Marks: 70  
Sessionals: 30

UNIT -I

UNIT -II

UNIT -III

UNIT -IV

UNIT -V
Tools for PCB Design and Layout

TEXT BOOKS:

REFERENCES:
ELECTIVE-I

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Credits: 4
Max. Marks: 70
Sessionals: 30

Subject Code: MTES-6(b)
I-Semester

Common with M.Tech (VLSI (MTVL -11)

UNIT-I
Programmable Logic Devices: ROM, PLA, PAL, PLD, PGA – Features, programming, applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT-II
CPLDs: programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD’s – CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST’s Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT-III
FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs , Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT & T – ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s – ACT- 1,2,3 and their speed performance.

UNIT-IV
Finite State Machines (FSM): Top down Design – State Transition Table, state assignments for FPGAs, Realization of state machine charts with a PAL. Alternative realization for state machine chart using microprogramming. Linked state machines. Encoded state machine. Architectures centered around non-registered PLDs, Design of state machines centered around shift registers, One Hot machine, Petrinets for state machine – Basic concepts and properties, Finite state machine – case study.

UNIT-V
Design Methods and System Level Design: One – Hot Design method, Use of ASMs in One – Hot Design Method, Applications of One-Hot Design Method, Extended Petri-nets for parallel controllers, Meeta stability, Synchronization, Complex design using shift registers. Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

UNIT-VI
Case studies: Design consideration using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.
TEXT BOOKS:
1. Field Programmable Gate Array Technology- S.Trimberger, Edr.1994, Kluwer Academic Publications,

REFERENCE:
2. Field programmable Gate Array, S.Brown, R.J.Francis, J.Rose, Z.G.Vranesic, 2007, BSP
ELECTIVE-I

DIGITAL DATA COMMUNICATIONS

Credits: 4
Max. Marks: 70
Sessionals: 30

Subject Code: MTES-6(c)
I-Semester

UNIT –I
Digital Modulation Techniques: FSK, MSK, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK Methods, Bandwidth efficiency, Carrier recovery, Clock recovery.

UNIT- II
Data Communication Methods and Protocols: Data Communication Circuit, point-to-point, Multi-point configurations and Topologies, transmission modes, 2-wire and 4-wire operations, Codes, Error detection methods, Error correction methods, Character synchronization. Asynchronous protocols, Synchronous protocols, Bisync Protocol, SDLC, HDLC-Frame format, Flow control and error control.

UNIT- III
Switching Techniques: Circuit Switching, Message Switching and Packet Switching principles, Virtual circuit and datagram techniques, X.25 and frame relay.

UNIT- IV

UNIT- V
Digital Multiplexing: TDM, T1 carrier system, CCITT-TDM carrier system, CODEC chips, Digital hierarchy, Line Encoding, Frame Synchronization. Multiplexers, Statistical multiplexer, Concentrator, front-end communication processor, Digital PBX, long haul communication with FDM, Hybrid data.

UNIT- VI

TEXT BOOKS:
2. William Stallings “Data and Computer Communications”, 7/e, PEI.

REFERENCES:
HDL PROGRAMMING LAB

Subject Code: MTES -7
I-Semester

Credits: 2
Max. Marks: 50
Sessionals: 50

Common with M.Tech (VLSI (MTVL -7))

1. Basic Gates
2. Adders
3. Subtractors
4. Full Adder using Two Half Adders
5. Decoders
6. 4 Bit Binary Adders
7. Multiplexers
8. Encoders
9. Demultiplexers
10. Comparators
11. Flip Flops
12. Counters
13. Shift Registers
14. Mealy & Moore Machine for sequence detector
15. Implementation of ALU
UNIT-I:
Programming on Linux Platform
System calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root file System, Busy Box.

UNIT-II:
Operating System Overview: Processes, Tasks, Threads, Multi Threading, Semaphore, Message Queue.

UNIT-III:
Introduction to Software Development Tools:
GNU GCC, make, gdb, static and dynamic linking, C Libraries, Compiler Options, Code Optimization Switches, lint, code profiling tools.

UNIT IV:
Interfacing Modules:
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, open CV for machine vision, Audio signal processing.

UNIT V:
Networking Basics:
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SBH, firewall, network security.

UNIT VI:
IA32 Instruction Set: Application Binary Interface, Exception and Interrupt Handling, Interrupt Latency, Assemblers, Assembler Directives, Macros, Simulation and debugging Tools.

TEXT BOOKS:

REFERENCE BOOKS:
2. The Design of the UNIX Operating System by Maurice J.Bach Prentice-Hall
3. UNIX Network programming by W.Richard Stevens
4. Assembly Language for X86 Processors by Kip R.Irvine
UNIT-I
The VHDL Design and combinational and Sequential Logic Design (Using VHDL)
Structural design elements, data flow design elements, behavioral design elements, and time dimension and simulation synthesis. Decoders, encoders, three state devices, multiplexers and Demultiplexers, Code Converters, EX-OR gates and parity circuits, comparators, adders & Subtractors, ALUs, Combinational multipliers. VHDL codes for the above ICs Barrel shifter, comparators, floating point encoder, dual priority encoder, Latches and flip-flops, PLDs, counters, shift register and their VHDL models, synchronous design methodology, impediments to synchronous design.

UNIT-II
Introduction to Verilog, Language Constructs and Conventions
Introduction, Keywords, Identifiers, Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches. White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT-III
Gate Level Modeling
Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

UNIT-IV
Behavioral Modeling
Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow, if and if-else constructs, assign-design construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT-V
Modeling at Data Flow Level and Switch Level Modeling
Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.
UNIT-VI

System Tasks, Functions, and Compiler Directives and Digital Design with SM Charts

Text Books

References:
UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESSING
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES AND EXECUTION
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing. Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT IV
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS AND FFT ALGORITHMS
The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.
UNIT VI
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

REFERENCES:
LOW POWER VLSI DESIGN

Subject Code: METS-12
II- Semester

Credits: 4
Max. Marks: 70
Sessionals: 30

Common with M.Tech (VLSI (MTVL-12))

UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

UNIT III
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT IV
CMOS AND BI-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance evaluation.

UNIT V
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free BiCMOS, Digital circuit operation and comparative Evaluation.

UNIT VI
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS:

REFERENCES:
2. CMOS Digital ICs Sung-mokang and yusuf leblebici, 3rd edition TMH 2003(Chapter 11)
3. VLSI DSP Systems, Parhi, John Wiley & sons, 2003(Chapter 17)
UNIT-I
Overview of Architecture and microcontroller Resources

UNIT-II
8051 Family Microcontrollers Instruction Set
Basic assembly language programming – Data transfer instructions – Data and Bit manipulation instructions – Arithmetic instructions – Instructions for Logical operations on the ‘Bytes’ among the Registers, Internal RAM, and SFRs – Program flow control instructions – Interrupt control flow.

UNIT-III
Real Time Control and Timers
Interrupt handling structure of an MCU – Interrupt Latency and Interrupt deadline – Multiple sources of the interrupts – Non-maskable interrupt sources – Enabling or Disabling of the sources – Polling to determine the Interrupt source and assignment of the priorities among them – Interrupt structure in Intel 8051. Programmable Timers in the MCUs – Free running counter and real time control – Interrupt interval and density constraints.

UNIT-IV
Systems Design

UNIT V
Real Time Operating System and Arm 32 Bit MCUs

UNIT VI
Microcontroller Based Industrial Applications
TEXT BOOKS:

REFERENCE BOOKS:
ELECTIVE-II

SYSTEM MODELLING & SIMULATION

Credits: 4
Max Marks: 70
II-SEMESTER

Common with M.Tech (VLSI (MTVL-10))

UNIT-I
Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT-II
SIMULATION SOFTWARE:
Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT-III
BUILDING SIMULATION MODELS AND MODELING TIME DRIVEN SYSTEMS
Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility. Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT-IV
EXOGENOUS SIGNALS AND EVENTS

UNIT-V
EVENT DRIVEN MODELS
Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT-VI
SYSTEM OPTIMIZATION
System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodology.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT I

UNIT II
Image Enhancement and Restoration:

UNIT III
Image Encoding: Objective and subjective Fidelity Criteria, the encoding process, the Mapping, the Quantizer and the Coder, Contour Encoding, Run length Encoding, Image Encoding relative to a Fidelity Criterion, Differential Pulse Code Modulation, Transform Encoding.

UNIT IV

UNIT V
Image Segmentation: The Detection of discontinuities, point line and Edge detection, Gradient operators, combined detection, thresholding.

UNIT VI
Image Representation: Representation schemes, chain codes, polygon Approximation, Boundary Descriptors, Simple descriptors, shape number, Fourier Descriptors. Image construction from projections: Random transforms, Convolution/ filter back Projection

TEXT BOOKS:

REFERENCES:
1. Rosefeld & Kak AC, Digital picture processing Academic Press INC.
ELECTIVE-II

COMPUTER AND COMMUNICATION NETWORKS

 Credits: 4
 Max. Marks: 70
II- Semester
 Common with M.Tech (RADAR AND MICROWAVE ENGINEERING (MTRM-12(b)))

UNIT-I

UNIT-II
Transmission Media and Digital Signaling, Analog vs. Digital Transmission, Nyquist and Shannon Limits, Digital or Analog Data to Digital Signals.

UNIT-III
Wireless Communication, Advances in cellular, personal communications systems (PCS), global system for mobile communications (GSM), wireless LANs - applications, satellites, and fixed wireless networks.

UNIT-IV
Error Detection and CRC Polynomial Codes. Data Link Control, Stop & Wait, Sliding Window ARQ, Go-back-N, Selective Reject.

UNIT-V
Data Link Layer Protocols and Multiplexing, HDLC, LAP-B, ARPANET DLC, Frequency and Time Division Multiplexing.

UNIT-VI
Circuit Switching and Packet Switching, Digital Switching Concepts, Packet Switching principles, Virtual Circuits and Datagrams, X.25, Frame and Cell Relay, ATM.

TEXT BOOKS:

REFERENCE BOOKS:
EMBEDDED SYSTEM LAB

Subject Code: MTES-15
II- Semester

Credits: 2
Max. Marks: 50
Sessionals: 50

Note: Minimum of 6 programs from Part-I and 6 programs from Part-II are to be conducted.

PART-I:
The following programs are to be implemented on ARM processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly program to configure and control General Purpose Input/output (GPIO) Port pins.
3. Write an Assembly Programs to read digital values from external peripherals and execute them with the Target Board.
4. Program for reading and writing of a file.
5. Program to demonstrate Time delay program using built in Timer/ Counter feature on IDE environment.
6. Program to demonstrate a simple interrupt handler and setting up a timer.
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment.
10. Program to displaying a message in a 2 line x 16 characters LCD display and verify the result in debug terminal.

PART-II:
Write the following programs to understand the use of RTOS with ARM Processor on IDE environment using ARM Tool chain and library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task.
3. Write an application that Demonstrate the interruptible ISRs (Require timer to have higher Priority than external interrupt button)
4. a) Write an application to Test message queues and memory blocks.
   b) Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings.
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mail box by one task and reading the message from mail box from another task.
9. Sending message to PC through serial port by three different tasks on priority Bases.
10. Basic Audio Processing on IDE environment.
III SEMESTER:

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Project work to be submitted before the end of 3rd Semester and it will be evaluated by a committee consisting of Chairman, Board of Studies, Head of the Department and thesis guide in the AUCE(A) and in the Affiliated Colleges Thesis (Part I) will be evaluated by concerned Head of the Department and thesis guide of their respective colleges.

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IV Semester:

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Thesis work is for a period of SIX months in Industry/Department. The students are required to submit their thesis in two/three phases. Thesis is evaluated by a committee consisting of an external member from reputed institution, HOD/ Chairman BOS and thesis Guide.